REMARKS

By this amendment, no claims have been amended, cancelled, or added. Accordingly, claims 28-30 are currently pending in the application, of which claims 28 and 30 are independent claims.

The specification has been amended to correct certain typographical errors. Applicant respectfully submits that the above corrections do not add new matter to the application and are fully supported by the specification.

Entry of the Remarks is respectfully requested because entry of Remarks places the present application in condition for allowance, or in the alternative, better form for appeal. In view of the following Remarks, Applicants respectfully request reconsideration and timely withdrawal of the pending rejections for the reasons discussed below.

Rejections Under 35 U.S.C. § 103

Claims 28 and 29 stand rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over Japanese Patent No. 02-179977 issued to Mishima et al. ("Mishima"), in view of Japanese Patent No. 06-77483 issued to Kaneko ("Kaneko") and U.S. Patent No. 5,354,700 issued to Huang et al. ("Huang"). Applicants respectfully traverse this rejection for at least the following reasons.

Claim 28 describes a thin film transistor array panel:

> A thin film transistor array panel, comprising:
> a plurality of pixels defined by gate lines and data lines;
> and
> a plurality of thin film transistors and pixel electrodes formed at the pixel and electrically connected to the gate lines and the data lines,

> wherein thin film transistors have a semiconductor layer and an ohmic layer, said semiconductor layer having a double-layered structure with a lower layer and an upper layer made of amorphous silicon layers which have different band gaps.

Mishima fails to teach all of the features of claim 28 of the present invention. As stated by the Examiner in the Office Action, Mishima does not show the semiconductor layer comprising a double-layered structure with an upper aSi layer with a lower band gap than a lower aSi layer.

The secondary references Kaneko and Huang do not fill the deficiencies of the primary reference, Mishima. Kaneko merely describes a thin film transistor that comprises a first amorphous silicon film 3-a and a second amorphous silicon film 3-b. Kaneko does not teach that the upper layer and lower layer have different band gaps, as recited in claim 28.

Further, Huang describes an FET thin film transistor that is formed with a first polysilicon layer 35 and a second polysilicon layer 37. However, Huang does not teach a double-layered amorphous silicon structure in which the two layers have different band gaps, as recited in claim 28.

The Examiner alleged that Huang teaches a semiconductor layer with an upper layer having a lower band gap than the lower layer. The Applicant believes that all the cited references simply describe different thicknesses of the layers, but fail to teach the different band gaps.

The proposed combination of Mishima, Kaneko, and Huang all fail to teach "a double-layered structure with a lower layer and an upper layer made of amorphous silicon layers which have different band gaps" as recited in claim 28.

Claim 30 stands rejected under 35 U.S.C. § 103(a) as being allegedly unpatentable over U.S. Patent No. 6,548,828 issued to Nakanishi et al. ("Nakanishi") in view of U.S. Patent No. 6,057,896 issued to Rho et al. ("Rho") and U.S. Patent No. 5,202,572 issued to Kobayashi ("Kobayashi").

Claim 30 describes a thin film transistor array panel:

> A thin film transistor array panel, comprising:
> a plurality of pixels defined by gate lines and data lines;
> and
> a plurality of thin film transistors and pixel electrodes formed at the pixel and electrically connected to the gate lines and the data lines,
> wherein thin film transistors have a gate insulating layer, said gate insulating layer having a double-layered structure including a lower insulating layer and an upper insulating layer, wherein one of the insulating layers is composed of an organic insulating material, and the other is composed of at least one of amorphous silicon nitride and amorphous silicon oxide.

Nakanishi describes a thin film transistor, but fails to teach all the limitations of claim 30 of the present application. As stated by the Examiner in the Office Action, Nakanishi does not show the use of amorphous silicon nitride or an organic material as a gate insulating material. In addition, Nakanishi does not show the use of amorphous silicon oxide in the gate insulating layer. Instead, Nakanishi teaches the use of a silicon nitride film 23 and a silicon oxide film 24 to form a gate insulating film.

The secondary references, Kobayashi and Rho do not fill the deficiencies of the primary reference, Nakanishi. Kobayashi merely describes an amorphous silicon nitride layer 30, but fails to teach a double-layered structure, wherein one of the insulating layers is composed of an

organic insulating material and the other is composed of amorphous silicon nitride or amorphous silicon oxide, as recited in claim 30.

Further, Rho does not teach the deficiencies either. Rho merely teaches the use of a flowable organic insulating layer and a silicon nitride pattern that is formed between the gate electrode and the semiconductor layer. Therefore, it does not teach the gate insulating layer as recited in claim 30. Instead, Rho, in Fig. 8 and Col. 6, lines 51-56, describes the silicon nitride pattern that only covers the gate electrode. Thus, Rho does not fill the deficiencies of the primary reference, Nakanishi.

Thus, the proposed combination of Nakanishi, Kobayashi, and Rho fails to teach all of the features of claim 30 of the present invention.

Accordingly, Applicants respectfully request withdrawal of the 35 U.S.C. § 103(a) rejection of claims 28 - 30. Since the none of the other prior art of record, whether taken alone or in any combination, discloses or suggests all the features of the claimed invention, Applicants respectfully submit that independent claims 28 and 30, and all the claims that depend therefrom are allowable.

CONCLUSION

Applicants believe that a full and complete response has been made to the pending Office Action and respectfully submits that all of the stated objections and grounds for rejection have been overcome or rendered moot. Accordingly, Applicants respectfully submit that all pending claims are allowable and that the application is in condition for allowance.

Should the Examiner feel that there are any issues outstanding after consideration of this response, the Examiner is invited to contact the Applicants' undersigned representative at the number below to expedite prosecution.

Prompt and favorable consideration of this Reply is respectfully requested.

Respectfully submitted,

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Date: 10 June 2005

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